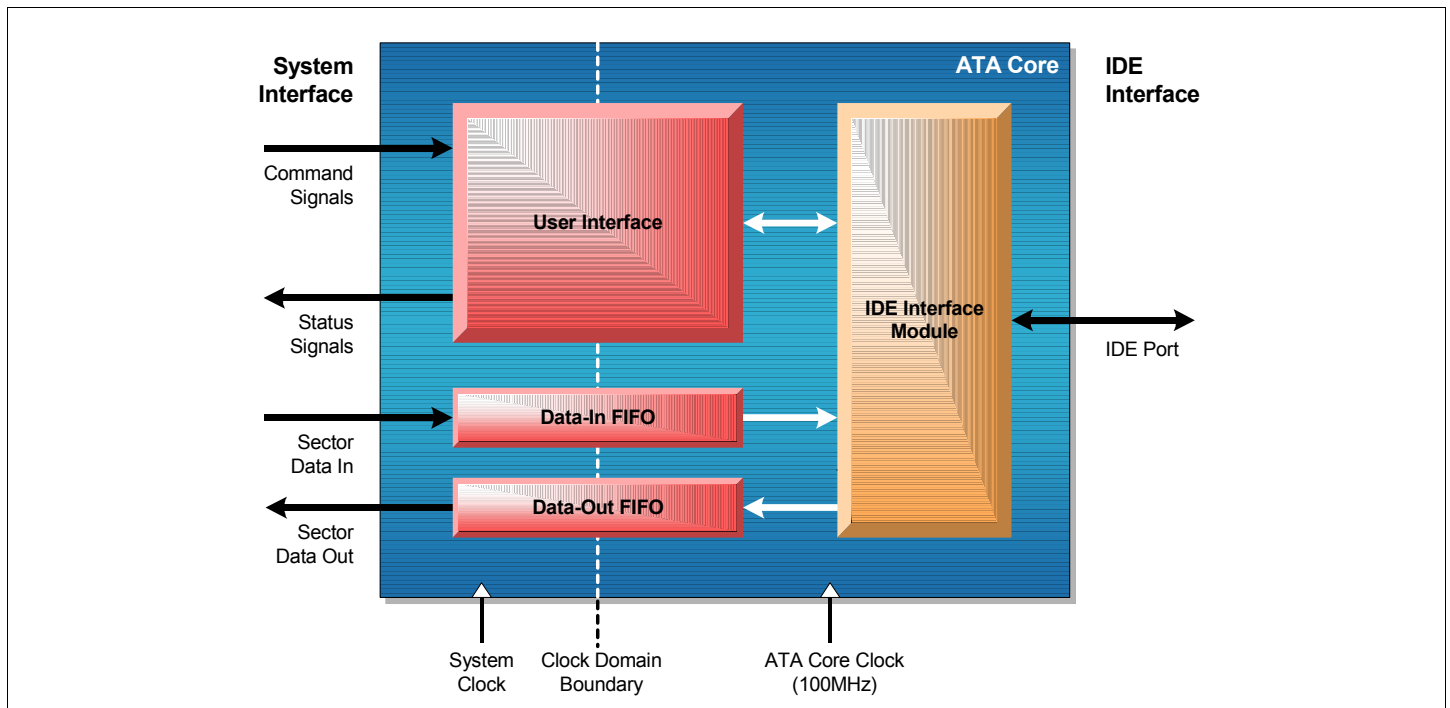


**ATA-4 / UDMA-33 IDE Core for Xilinx Devices**

The ATA-4 / UDMA-33 IDE Core is a drop-in ATA-Host IP core used for interfacing to an ATA-device. It handles all transactions on the IDE bus for various commands that are dispatched from the system. After a command is dispatched, the ATA-core executes the command on the ATA device. Once the command execution is completed, the final status is reported to the system side. At that time, the system can execute a new command. The ATA-4 core from Nuvation is available either as an encrypted Netlist or as a source code license.

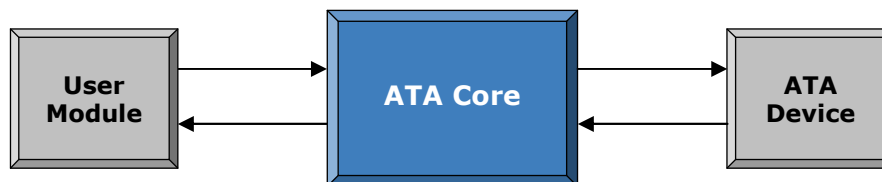
Features	Command Set
<ul style="list-style-type: none"> <li>ATA/ATAPI-4 standard compliant host</li> <li>UDMA-33 transfer speed capabilities (33 MB/s max transfer speed)</li> <li>RX and TX FIFOs for data transfer through the Core</li> <li>DMA/UDMA and PIO data transfers supported</li> <li>Dedicated signal for polling ATA-device status</li> <li>Dedicated signal for executing Software Reset command</li> <li>Two Clock domains: Core Clock and System Clock domains</li> <li>Dedicated system side input bus for writing data to the ATA device</li> <li>Dedicated system side output bus for data read from the ATA device</li> <li>Required Core Clock Speed: 100MHz</li> <li>Available PIO Modes: 0 and 4</li> <li>Number of ATA devices supported on the IDE Bus: 1</li> </ul> <p><b>Target Device Families: Spartan 3/3E, Virtex II/IIPro/4</b></p> <ul style="list-style-type: none"> <li>Number of Slices: <b>911</b></li> <li>Number of Memory Bits: <b>8192</b></li> </ul> <p>ISE Version: 6.2i</p>	<ul style="list-style-type: none"> <li>Check Power Mode</li> <li>Identify Device</li> <li>Idle</li> <li>Idle Immediate</li> <li>Initialize Device Parameters</li> <li>Read Verify Sector(s)</li> <li>Seek</li> <li>Set Features</li> <li>Set Multiple Mode</li> <li>Sleep</li> <li>Standby</li> <li>Standby Immediate</li> <li>Execute Device Diagnostic</li> <li>Read DMA</li> <li>Read Multiple</li> <li>Read Sector(s)</li> <li>Write DMA</li> <li>Write Multiple</li> <li>Write Sector(s)</li> </ul>

**System Architecture**



Nuvation ATA-4 / UDMA-33 IDE Core Architecture for Xilinx Devices

ATA I/O Signal List



The following table lists I/O signals for the ATA Core. Input and output directions are with respect to the ATA Core.

Internal Signal Name	I/O	Description
<b>General Signals</b>		
core_clk	I	ATA Core Global Clock (TBD MHz)
core_reset_n	I	ATA Core Global Reset
<b>ATA Bus</b>		
CS0_n	O	Chip Select 0
CS1_n	O	Chip Select 1
DD[15:0]	I/O	Data Bus
DASP_n		Device active or slave present
DA[2:0]	O	Device Address
DMACK_n	O	DMA Acknowledge
DMARQ	I	DMA Request
INTRQ	I	Interrupt Request
DIOR_n	O	3 purpose signal: - I/O read - DMA ready during Ultra DMA data in bursts - Data strobe during Ultra DMA data out bursts
IORDY	I	3 purpose signal: - I/O ready - DMA ready during Ultra DMA data our bursts - Data strobe during Ultra DMA data in bursts
DIOW_n	O	Dual Purpose Signal: - I/O write - Stop during Ultra DMA data bursts
PDIAG_n		Dual Pupose Signal: - Passed diagnostics - Cable assembly type identifier
RESET_n	O	Reset
<b>Local Side Interface</b>		
<b>General Signals</b>		
sys_clk	I	System-side (User) Clock
sw_reset	I	Signal is asserted to initiate a software reset of the device.
read_all_status	I	A 0-to-1 transfer initiates a read of all current status registers. Must be re-set to 0 again before a subsequent 'read all status' request.
core_busy	O	This signal indicates the Core's current status - whether it is busy or idle.
<b>Input ATA Transactions</b>		
Command Path (control path)		
feature[7:0]	I	Feature field of the task file (command block)
sector_count[7:0]	I	Sector Count field of the task file
sector_number[7:0]	I	Sector Number field of the task file
cylinder_low[7:0]	I	Cylinder Low field of the task file
cylinder_high[7:0]	I	Cylinder High field of the task file

Internal Signal Name	I/O	Description
device_head[7:0]	I	Device Head field of the task file
command_dav	O	When high, the ATA Core can accept a new command
command[7:0]	I	Command field of the task file
command_valid	I	Initiates the Command. Qualifies the following buses: feature, sector_count, sector_number, cylinder_low, cylinder_high, device_head, command and transaction_id_in
transaction_id_in[3:0]	I	User Field for identifying various transactions. This value will be returned to the user on the "transaction_id_out" bus when the command has been processed. [for future use]
command_error	O	This signal is high for one cycle after an unsupported command is dispatched or if the core receives a new command when it is busy.
<b>Input Data Path (data path)</b>		
sector_data_in_dav	O	Core can accept sector data
sector_data_in_valid	I	Input Data is Valid
sector_data_in[15:0]	I	Data to be written to the storage media (qualified by sector_data_valid)
sector_data_overflow	O	This signal is asserted for every cycle that data was lost in the sector_data FIFO.
<b>Output ATA Transactions</b>		
<b>Status Path (control path)</b>		
error[7:0]	O	Error Field of command results
status_sector_count[7:0]	O	Sector Count field of the task file (if required)
status_sector_number[7:0]	O	Sector Number field of the task file (if required)
status_cylinder_low[7:0]	O	Cylinder Low field of the task file (if required)
status_cylinder_high[7:0]	O	Cylinder High field of the task file (if required)
status_device_head[7:0]	O	Device Head field of the task file (if required)
status[7:0]	O	Status Field of command results
status_valid	O	This signal indicates when the appropriate status signals are valid. [for future use]
transaction_id_out[3:0]	O	When valid, this signal contains the same value that was placed on the "transaction_id_in" bus upon command initiation.
<b>Output Data Path (data path)</b>		
sector_data_out_dav	O	When high, this signal indicates whether there is data available for the user to read.
sector_data_out_ena	I	When high, and if data available, this signal causes data to be placed on the "sector_data_out" bus on a cycle-by-cycle basis.
sector_data_out_valid	O	This signal qualifies the following bus: sector_data_out
sector_data_out[15:0]	O	The data read from storage media

NOTE: The Nuvation ATA-4 IP Core can be customized to customer requirements. For example, the signal list may be altered to support extra functionality provided by ATAPI commands for a Packet interface / Packet command.