

OVERVIEW

The ATA-5 / UDMA-66 IDE OPB Core is a drop-in ATA-Host IP core used for interfacing to an ATA-device. The core has all connections to interface to an OPB bus and IDE bus. The OPB bus is used for writing to and reading from the taskfile registers needed for the data transactions. It is also used to read/write the data from/to the ATA hard drive when a transaction is initiated. The core handles all transactions on the IDE bus for various commands that are dispatched from the system. The core integrates with Xilinx PowerPC or MicroBlaze processors in the EDK Tool flow.

TARGET DEVICES

Xilinx Spartan-3/3E
Xilinx Virtex-II / Pro
Xilinx Virtex-4
Xilinx Virtex-5

Slice FFs 1250
BRAMs 2

FEATURES

- ATA/ATAPI-4 standard compliant host
- UDMA-66 transfer speed capabilities (33 MB/s max transfer speed)
- RX and TX FIFOs for data transfer through the Core
- DMA/UDMA and PIO data transfers supported
- Dedicated signal for executing Software Reset command
- Two Clock domains: Core Clock and System Clock domains
- Dedicated system side input bus for writing data to the ATA device
- Dedicated system side output bus for data read from the ATA device
- Required Core Clock Speed: 100MHz
- Available PIO Modes: 0 and 4
- Number of ATA devices supported on the IDE Bus: 1

COMMAND SET

- Check Power Mode
- Identify Device
- Idle
- Idle Immediate
- Initialize Device Parameters
- Read Verify Sector(s)
- Seek
- Set Features
- Set Multiple Mode
- Sleep
- Standby
- Standby Immediate
- Execute Device Diagnostic
- Read DMA
- Read Multiple
- Read Sector(s)
- Write DMA
- Write Multiple
- Write Sector(s)

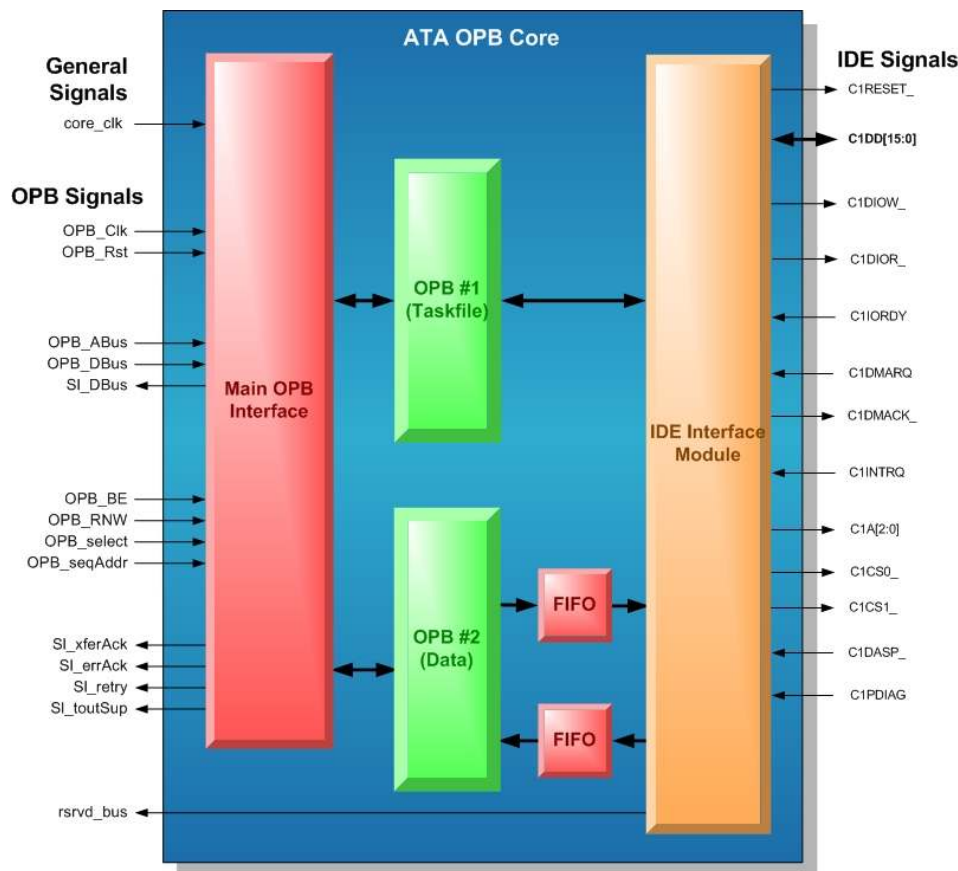
LICENSING

The ATA-5 OPB core from Nuvation is available either as an encrypted Netlist or as a source code license.

The licensing package includes:

- Core
- User Guide
- Support Package
- 1-Year Warranty

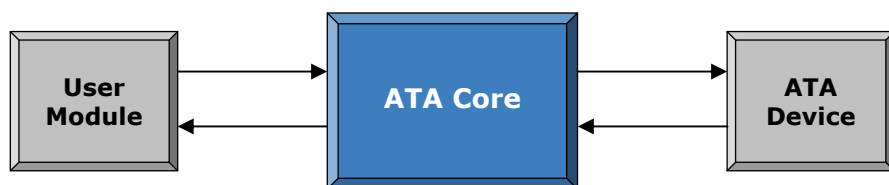
Nuvation's User Guide provides detailed step-by-step instructions for quick and easy integration.



ATA-5 OPB Block Diagram

SIGNAL LIST

The following table lists I/O signals for the ATA Core. Input and output directions are with respect to the ATA Core.



INTERNAL SIGNAL NAME	I/O	DESCRIPTION
GENERAL SIGNALS		
core_clk	I	Core Clock (100 MHz)
ON-CHIP PERIPHERAL BUS (OPB)		
OPB_ABus[31:0]	I	OPB address bus
OPB_BE[3:0]	I	OPB byte enable This bus is NOT used. Both taskfile (OPB #1) and data (OPB #2) assume there is valid data on the least-significant bytes for every write.
OPB_DBus[31:0]	I	OPB data bus Input data for OPB slave.
OPB_RNW	I	OPB read/not write 1 means the OPB slave is asked to output data on the SI_DBus . 0 means the OPB slave is asked to take in data from the OPB_DBus .
OPB_select	I	OPB select To validate OPB input signals and denote when an OPB transfer is in progress.
OPB_seqAddr	I	OPB sequential address This signal is NOT being used
SI_DBus[31:0]	O	Slave data bus Output data for OPB slave.
SI_errAck	O	Slave error acknowledge This signal is NOT being used, and is stuck at ground (GND). This is because OPB #1 is guaranteed to always be able to receive the taskfile command. OPB#2 is also always guaranteed to either read/write successfully (SI_xferAck), or to have a retry when the FIFO cannot be read/written (SI_retry).
SI_retry	O	Slave retry This signal is only used by the data sub-interface (OPB #2). The signal is triggered when the OPB slave is being asked to write to a full FIFO or to read from an empty FIFO.
SI_toutSup	O	Slave timeout suppress This signal is NOT being used, and is stuck at ground (GND). This is because both OPB #1 and OPB #2 sub-interfaces guarantee that either the SI_xferAck or the SI_retry signal will be triggered within 16 clock cycles.
SI_xferAck	O	Slave transfer acknowledge This signal is asserted for one clock cycle to denote the successful completion of the current OPB command execution.
RESERVED STATUS BUS		
rsrvd_bus[15:0]	O	Reserved for future use. Leave unconnected.

INTERNAL SIGNAL NAME	I/O	DESCRIPTION
IDE INTERFACE		
C1DD[15:0]	I/O	IDE Data Bus
C1RESET_	O	IDE Reset (active low)
C1DIOR_	O	IDE 3 purpose signal: <ul style="list-style-type: none"> I/O read (active low) DMA ready during Ultra DMA data in bursts Data strobe during Ultra DMA data out bursts In the ATA specification, this signal is called DIOR- ; HDMARDY- ; HSTROBE
C1IORDY	I	IDE 3 purpose signal: <ul style="list-style-type: none"> I/O ready DMA ready during Ultra DMA data out bursts Data strobe during Ultra DMA data in bursts In the ATA specification, this signal is called IORDY ; DDMARDY- ; DSTROBE
C1DIOW_	O	IDE Dual Purpose Signal: <ul style="list-style-type: none"> I/O write (active low) Stop during Ultra DMA data bursts In the ATA specification, this signal is called DIOW- ; STOP
C1DMACK_	O	IDE DMA Acknowledge
C1DMARQ	I	IDE DMA Request
C1INTRQ	I	IDE Interrupt Request
C1CS0_	O	IDE Chip Select 0 (active low)
C1CS1_	O	IDE Chip Select 1 (active low)
C1DA[2:0]	O	IDE Device Address
C1DASP_	I	IDE Device active or slave present
C1PDIAG	I	IDE Dual Purpose Signal: <ul style="list-style-type: none"> Passed diagnostics Cable assembly type identifier In the ATA specification, this signal is called PDIAG- ; CBLID- This signal is reserved for future use.

NOTE: The Nuvation ATA-5 OPB IP Core can be customized to customer requirements. For example, the signal list may be altered to support extra functionality provided by ATAPI commands for a Packet interface / Packet command.

EXTENSION MODULE	CONTACT
<p>An extension module for 48-bit Line Bit Addressing (LBA) is available upon request (LBA-48 is a component of the ATA-6 specification for addressing HDDs >137GB).</p>	<p>EMAIL IP@NUVATION.COM WEB NUVATION.COM TEL 408.228.5580 FAX 408.228.5590</p>