

ATA-5 Host Controller with PLB interface for Xilinx Devices

The ATA-5 / UDMA-66 IDE Core is a drop-in ATA-Host IP core used for interfacing to an ATA-device. It handles all transactions on the IDE bus for various commands that are dispatched from the system. After a command is dispatched, the ATA-core executes the command on the ATA device. Once the command execution is completed, the final status is reported to the system side. At that time, the system can execute a new command.

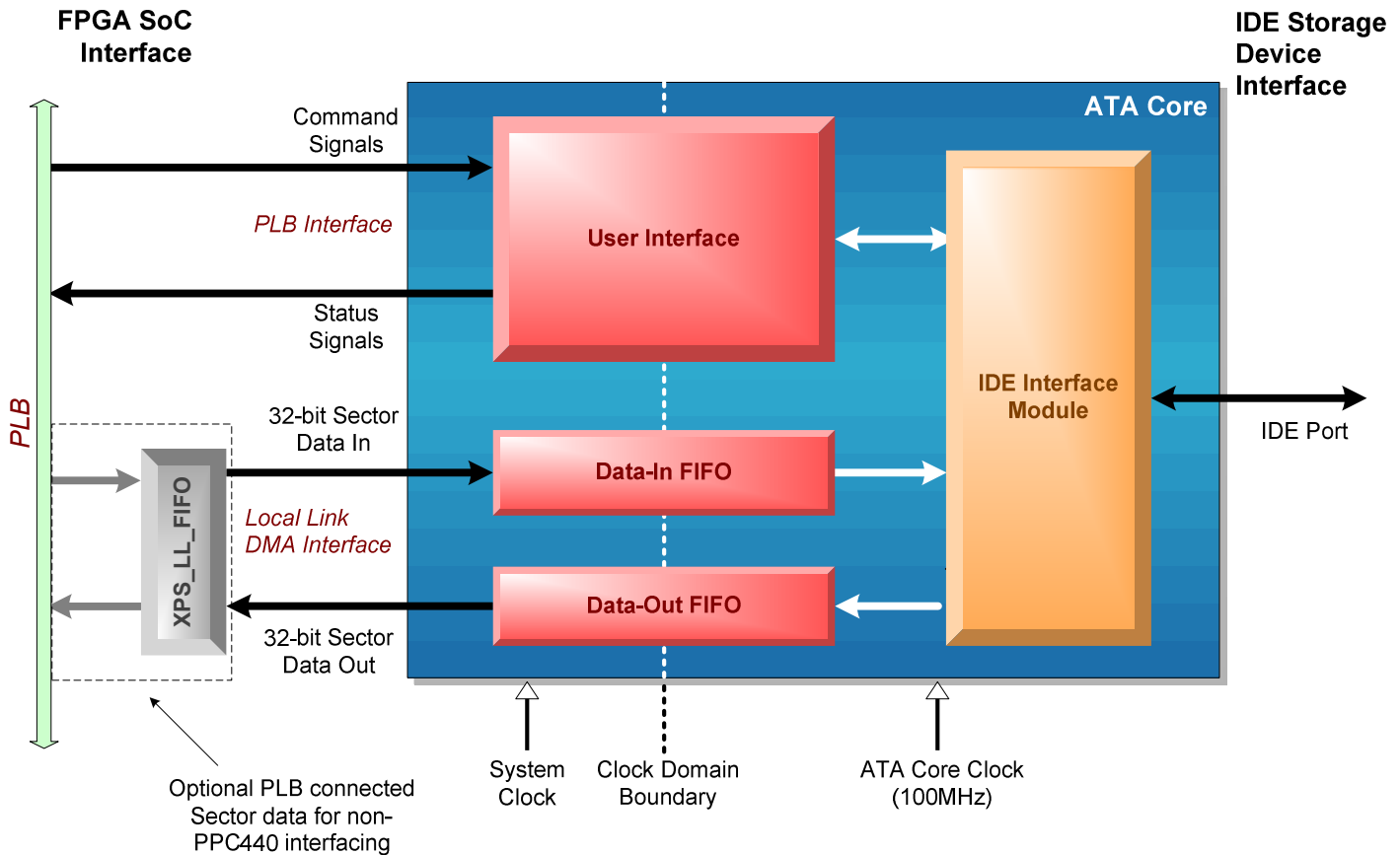
The ATA-5 core features a PLB interface for use in all Xilinx FPGA devices. Nuvation's ATA-5 controller also connects directly to the Local Link DMA ports of the PPC440 specifically for Virtex-5 FXT devices. In devices other than Virtex-5 FXT, the core should be used with the Xilinx XPS_LL_FIFO component to connect the ATA-5 local Link interface to PLB.

Applications often include controllers for HDDs, Compact Flash, and Solid State Disk Drives. Utilizing available FPGA resources can reduce PCB real estate and product cost. Multiple instantiations of the ATA core can be implemented for RAID-type architectures.

The ATA-5 core from Nuvation is available under IP core license agreements. Licensee Deliverables include the Netlist, Verilog Test Bench, Detailed User Guide, Support, and Warranty. Extended Support, Extended Warranty, and Source Code licenses are also available.

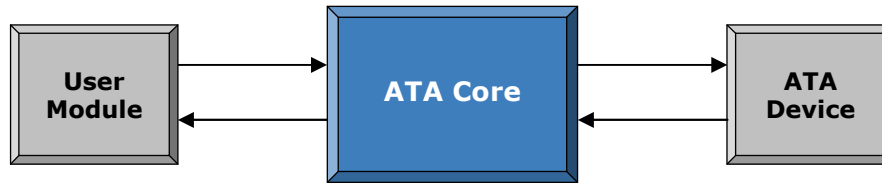
Features	Command Set
<ul style="list-style-type: none"> • ATA-5 standard compliant host • UDMA-66 transfer speed capabilities (66 MB/s max transfer speed) • RX and TX FIFOs for data transfer through the Core • DMA/UDMA and PIO data transfers supported • Dedicated signal for polling ATA-device status • Dedicated signal for executing Software Reset command • Two Clock domains: Core Clock and System Clock domains • PLB interface for command and status • LocalLink DMA interface for writing data to the ATA device • LocalLink DMA interface for reading data from the ATA device • Required Core Clock Speed: 100MHz • Available PIO Modes: 0 and 4 • Number of ATA devices supported on the IDE Bus: 1 • Optional LBA-48 support (module included upon request) <p>Target Device Family: Xilinx Spartan 3, Virtex II/Pro with PLB</p> <ul style="list-style-type: none"> • Number of Slices: 911 • Number of Memory Bits: 8192 <p>Target Device Family: Xilinx Virtex-5 with PLB and LocalLink</p> <ul style="list-style-type: none"> • Number of Slices: 1502 • Number of Memory Bits: 8192 	<ul style="list-style-type: none"> • Check Power Mode • Identify Device • Idle • Idle Immediate • Initialize Device Parameters • Read Verify Sector(s) • Seek • Set Features • Set Multiple Mode • Sleep • Standby • Standby Immediate • Execute Device Diagnostic • Read DMA • Read Multiple • Read Sector(s) • Write DMA • Write Multiple • Write Sector(s)

ATA-5 Host Controller Block Diagram



Nuvation ATA-5 Host Controller IP Core, PLB for Xilinx version

ATA I/O Signal List



The following table lists I/O signals for the ATA Core. Input and output directions are with respect to the ATA Core.

Internal Signal Name	I/O	Description
General Signals		
core_clk	I	Core clock (100 MHz)
Processor Local Bus (PLB)		
iSPLB_CLK	I	PLB System Clock.
iSPLB_RST	I	PLB System Reset.
iPLB_ABUS[31:0]	I	PLB Address Bus.
iPLB_PAVVALID	I	PLB primary address valid indicator.
iPLB_MASTERID	I	PLB current Master Identifier.
iPLB_RNW	I	PLB Read Not Write.
iPLB_BE[3:0]	I	PLB Byte Enables. Not used.
iPLB_WRBURST	I	PLB Burst Write Transfer indicator.
iPLB_RDBURST	I	PLB Burst Read Transfer indicator.
iPLB_SIZE[3:0]	I	PLB Transfer Size.
iPLB_TYPE[2:0]	I	PLB Transfer Type.
iPLB_WRDBUS[pSPLB_DWIDTH-1:0]	I	PLB Write Data Bus.
iPLB_MSIZE[1:0]	I	PLB Master Data Bus Size.
oSL_ADDRACK	O	Slave Address Acknowledge.
iPLB_SIZE[1:0]	O	Slave Data Bus Size.
oSL_WAIT	O	Slave Wait indicator.
oSL_REARBITRATE	O	Slave re-arbitrate indicator.
oSL_WRDACK	O	Slave Write Data Acknowledge.
oSL_WRCOMP	O	Slave Write Transfer Complete Indicator.
oSL_WRBTERM	O	Slave Terminate Write Burst Transfer.
oSL_RDBUS[pSPLB_DWIDTH-1:0]	O	Slave Read Data Bus.
oSL_RDDACK	O	Slave Read Data Acknowledge.
oSL_RDCOMP	O	Slave Read Transfer Complete indicator.
oSL_RDBTERM	O	Slave Terminate Read Burst Transfer.
oSL_RDWDADDR[3:0]	O	Slave Read Word Address.
RX Local Link DMA Interface (Host Write Data Interface)		
iSRC_RDY_n	I	Source (Host) Ready. Active Low.
iSOF_n	I	Start of Frame. Active Low.
iEOF_n	I	End of Frame. Active Low.
iSOP_n	I	Start of Packet. Active Low.
iEOP_n	I	End of Packet. Active Low.
iREM[3:0]	I	Indication of Footer bytes when iEOP_n is asserted.
iDMA_DATA[31:0]	I	DMA Write data from Host.
oDST_RDY_n	O	Destination (ATA core) Ready. Active Low.
TX Local Link DMA Interface (Host Read Data Interface)		
iDST_RDY_n	I	Destination (Host) Ready. Active Low.
oSRC_RDY_n	O	Source (ATA core) Ready. Active Low.
oSOF_n	O	Start of Frame. Active Low.
oEOF_n	O	End of Frame. Active Low.
oSOP_n	O	Start of Packet. Active Low.
oEOP_n	O	End of Packet. Active Low.
oREM[3:0]	O	Footer Byte indicator when oEOP_n is asserted.
oDMA_DATA[31:0]	O	DMA Read Data to Host.

Internal Signal Name	I/O	Description
IDE Interface		
DD[15:0]	I/O	IDE Data Bus
RESET_	O	IDE Reset (active low)
DIOR_	O	IDE 3 purpose signal: <ul style="list-style-type: none"> I/O read (active low) DMA ready during Ultra DMA data in bursts Data strobe during Ultra DMA data out bursts In the ATA specification, this signal is called DIOR-; HDMARDY-; HSTROBE
IORDY	I	IDE 3 purpose signal: <ul style="list-style-type: none"> I/O ready DMA ready during Ultra DMA data our bursts Data strobe during Ultra DMA data in bursts In the ATA specification, this signal is called IORDY; DDMARDY-; DSTROBE
DIOW_	O	IDE Dual Purpose Signal: <ul style="list-style-type: none"> I/O write (active low) Stop during Ultra DMA data bursts In the ATA specification, this signal is called DIOW-; STOP
DMACK_	O	IDE DMA Acknowledge
DMARQ	I	IDE DMA Request
INTRQ	I	IDE Interrupt Request
CS0	O	IDE Chip Select 0 (active low)
CS1	O	IDE Chip Select 1 (active low)
DA[2:0]	O	IDE Device Address
DASP_	I	IDE Device active or slave present
PDIAG	I	IDE Dual Purpose Signal: <ul style="list-style-type: none"> Passed diagnostics Cable assembly type identifier In the ATA specification, this signal is called PDIAG-; CBLID- This signal is reserved for future use.
Status Signals		
oRDMAFIFO_EMPTY	O	Read DMA FIFO (Local Link TX interface) EMPTY indicator.
oRDMAFIFO_FULL	O	Read DMA FIFO (Local Link TX interface) FULL indicator.
oRDMAFIFO_USEDW [pRDMAFIFO_COUNTER_WD - 1 : 0]	O	No. of 32-bit words present in Read DMA FIFO. pRDMAFIFO_COUNTER_WD = log2(Length of Read DMA FIFO)
oWDMAFIFO_EMPTY	O	Write DMA FIFO (Local Link RX interface) EMPTY indicator.
oWDMAFIFO_FULL	O	Write DMA FIFO (Local Link RX interface) FULL indicator.
oWDMAFIFO_USEDW [pWDMAFIFO_COUNTER_WD - 1 : 0]	O	No. of 32-bit words present in Write DMA FIFO. pWDMAFIFO_COUNTER_WD = log2(Length of Write DMA FIFO)
oCOMMAND_ERROR	O	The signal becomes '1' if the last issued command is not supported by the ATA core.
oCOMMAND_DAV	O	This signal indicates that the core is ready to accept new command. This status can also be read by reading the Core State Status Register through the PLB interface.
oCORE_BUSY	O	Core Busy status signal. Indicates that the core is busy processing the last issued command or performing initialization protocol with the ATA device. A new command should only be issued when this signal is '0'. This status can also be read by reading the Core State Status Register through the PLB interface.
oSECTOR_DATA_IN_DAV	O	Indicates the RX Local Link DMA interface is ready to accept sector data to be written to the ATA device. This signal is equal to NOT (oDST_RDY_n).
oSECTOR_DATA_OUT_DAV	O	Indicates the availability of Read Sector data through the TX Local Link DMA interface. This signal is equal to NOT (oSRC_RDY_n).
oSECTOR_DATA_OUT_VALID	O	Indicates that the valid data is present at oDMA_DATA[31:0] port of TX Local Link interface.

NOTE: The Nuvation ATA-5 IP Core can be customized to customer requirements. For example, the signal list may be altered to support extra functionality provided by ATAPI commands for a Packet interface / Packet command.

ATA-5 Command Set

The following table outlines the currently supported ATA-5 command set. All of the mandatory (as stated in T13/1153D revision 18) commands are implemented by the Core.

Abbreviations used below:

ND: Non-data command

DM: DMA command – follows the DMA data transfer protocol

PI: PIO data in command – follows the PIO Data-In data transfer protocol

PO: PIO data out command – follows the PIO data-Out data transfer protocol

DD: Execute Device Diagnostic command and protocol

Command, and Type / Protocol	Description	Command Code
Non-Data Command		
Check Power Mode ND	Allows the host to determine the current power mode of the device. The command will not cause the power mode to change.	E5h
Identify Device ND	This command enables the host to receive parameter information from the device. The parameter data consists of 256 words, and contains data relevant to the device's capabilities and expectations.	ECh
Idle ND	Will place the device into an Idle state following a specified timeout period.	E3h
Idle Immediate ND	Will immediately place the device into an idle state – same as Idle, above, but without the timeout period.	E1h
Initialize Device Parameters ND	This command allows the host to set the number of logical sectors per track and the number of logical heads per logical cylinder for the current CHS translation mode.	91h
Read Verify Sector(s) ND	Similar to Read Sector(s) (below), the device will read the requested data. However, the data is not transferred to the host – it only has its integrity verified by the device.	40h
Seek ND	Allows the host to provide advance notice that data may be requested by the host in a subsequent command.	70h
Set Features ND	Allows the host to establish parameters that affect the execution of certain device features.	EFh
Set Multiple Mode ND	Establishes the block count for Read Multiple and Write Multiple commands.	C6h
Sleep ND	This command is the only way to cause the Device to enter sleep mode.	E6h
Standby ND	Will place the device into a Standby state following a specified timeout period.	E2h
Standby Immediate ND	Will immediately place the device into a Standby state – same as Standby, above, but without the timeout period.	E0h
Execute Device Diagnostic Commands		
Execute Device Diagnostic DD	This command shall perform the internal diagnostic tests implemented by the device.	90h
Data-In Commands (reads)		
Read DMA DM	Allows the host to read data using the DMA data transfer protocol.	C8h
Read Multiple PI	Requests a read of data from the device. The requested number of sectors of data is returned by the device to the host.	C4h
Read Sector(s) PI	Requests a read of data from the device. The sectors of data are returned by the device to the host.	20h
Data-Out Command (writes)		
Write DMA DM	Allows the host to write data using the DMA data transfer protocol.	CAh
Write Multiple PO	This command writes data to the device in blocks of sectors.	C5h
Write Sector(s) PO	This command writes from 1 to 256 sectors of data to the device, as specified in the command task file.	30h