

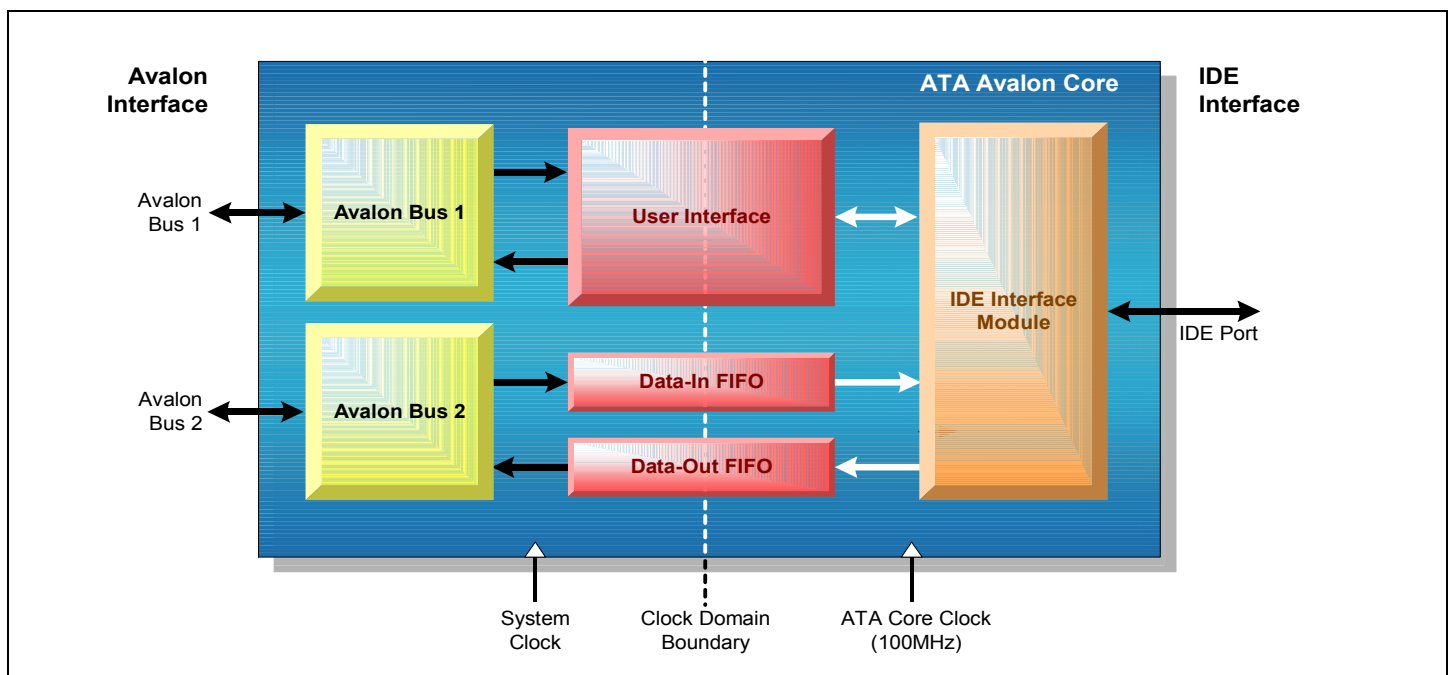
ATA-5 Avalon IP Core

The ATA-5 / UDMA-66 IDE Avalon Core is a drop-in ATA-Host IP core used for interfacing to an ATA-device. The core has all connections to interface to an Avalon bus and IDE bus. Two Avalon buses are used in the design. One bus controls writing to and reading from the taskfile registers needed for the data transactions. The second Avalon bus reads and writes the data to the ATA hard drive when a transaction is initiated. It handles all transactions on the IDE bus for various commands that are dispatched from the system.

The ATA-5 Avalon core from Nuvation is available either as an encrypted Netlist or as a source code license. This core is also available in Altera SOPC Builder for seamless integration into any design.

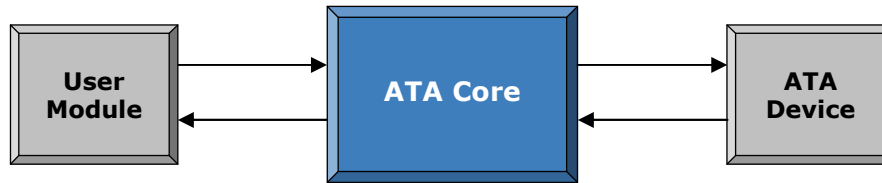
| Features | Command Set |
|--|--|
| <ul style="list-style-type: none"> • ATA/ATAPI-5 standard compliant host • UDMA-66 transfer speed capabilities (66 MB/s max transfer speed) • RX and TX FIFOs for data transfer through the Core • DMA/UDMA and PIO data transfers supported • Dedicated signal for polling ATA-device status • Dedicated signal for executing Software Reset command • Two Clock domains: Core Clock and System Clock domains • Dedicated system side input bus for writing data to the ATA device • Dedicated system side output bus for data read from the ATA device • Required Core Clock Speed: 100MHz • Available PIO Modes: 0 and 4 • Number of ATA devices supported on the IDE Bus: 1 <p>Target Device Family: Altera Cyclone</p> <ul style="list-style-type: none"> • Number of LE: 1056 • Number of Memory Bits: 8192 | <ul style="list-style-type: none"> • Check Power Mode • Identify Device • Idle • Idle Immediate • Initialize Device Parameters • Read Verify Sector(s) • Seek • Set Features • Set Multiple Mode • Sleep • Standby • Standby Immediate • Execute Device Diagnostic • Read DMA • Read Multiple • Read Sector(s) • Write DMA • Write Multiple • Write Sector(s) |

System Architecture



Nuvation ATA-5 Avalon Core Architecture for Altera Devices

ATA I/O Signal List



The following table lists I/O signals for the ATA Core. Input and output directions are with respect to the ATA Core.

| Internal Signal Name | I/O | Description |
|------------------------|-----|--|
| General Signals | | |
| clk | I | Clock |
| core_clk | I | 100 MHz Core clock |
| reset_n | I | Reset |
| Avalon Bus 1 | | |
| a1_read_n | I | Read data from taskfile register specified by the address and place value on readdata lines |
| a1_readdata[7:0] | O | Data read from taskfile registers |
| a1_write_n | I | Write data on writedata lines to taskfile register specified by the address |
| a1_writedata[7:0] | I | Data to be written to taskfile registers |
| a1_address[7:0] | I | Address of taskfile register to be written to or read from |
| a1_chipselect | I | The slave port should ignore all other Avalon signals unless chipselect is asserted |
| Avalon Bus 2 | | |
| a2_read_n | I | Read data from FIFO Out register specified by the address |
| a2_readdata[15:0] | O | Data read from taskfile registers |
| a2_write_n | I | Write data on writedata lines to FIFO In register specified by the address |
| a2_writedata[15:0] | I | Data to be written to taskfile registers |
| a2_address[7:0] | I | Address of taskfile register to be written to or read from |
| a2_chipselect | I | The slave port should ignore all other Avalon signals unless chipselect is asserted |
| a2_readyfordata | O | This signal indicates that the device can receive data |
| a2_dataavailable | O | This signal indicates that the device has data available |
| IDE Interface | | |
| C1DD[15:0] | I/O | Data Bus |
| C1RESET_ | O | Reset |
| C1DIOR_ | O | 3 purpose signal: <ul style="list-style-type: none"> ▪ I/O read ▪ DMA ready during Ultra DMA data in bursts ▪ Data strobe during Ultra DMA data out bursts |
| C1IORDY | I | 3 purpose signal: <ul style="list-style-type: none"> ▪ I/O ready ▪ DMA ready during Ultra DMA data our bursts ▪ Data strobe during Ultra DMA data in bursts |
| C1DIOW_ | O | Dual Purpose Signal: <ul style="list-style-type: none"> ▪ I/O write ▪ Stop during Ultra DMA data bursts |
| C1DMACK | O | DMA Acknowledge |
| C1DMARQ | I | DMA Request |
| C1INTRQ | I | Interrupt Request |
| C1CS0_ | O | Chip Select 0 |
| C1CS1_ | O | Chip Select 1 |
| C1DA[2:0] | O | Device Address |
| C1DASP_ | I | Device active or slave present |
| C1PDIAG | I | Dual Purpose Signal: <ul style="list-style-type: none"> ▪ Passed diagnostics ▪ Cable assembly type identifier |