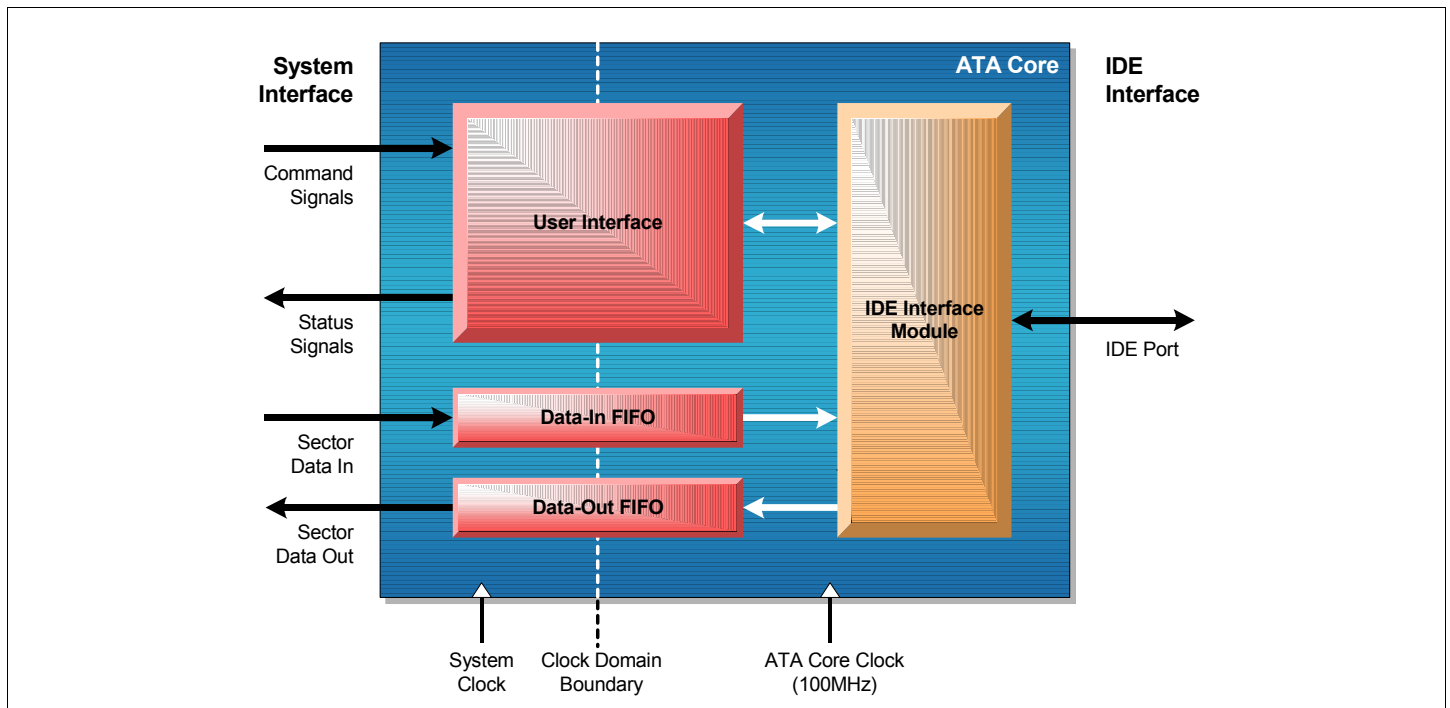


ATA-5 / UDMA-66 IDE Core for Xilinx Devices

The ATA-5 / UDMA-66 IDE Core is a drop-in ATA-Host IP core used for interfacing to an ATA-device. It handles all transactions on the IDE bus for various commands that are dispatched from the system. After a command is dispatched, the ATA-core executes the command on the ATA device. Once the command execution is completed, the final status is reported to the system side. At that time, the system can execute a new command. The ATA-5 core from Nuvation is available as either an encrypted Netlist or as a source code license.

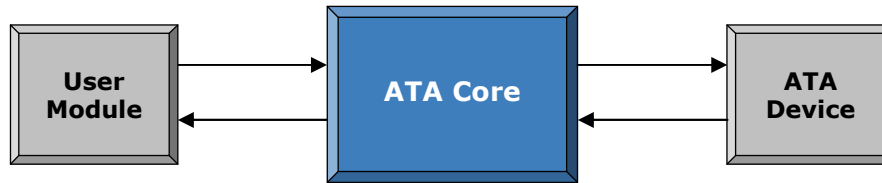
Features	Command Set
<ul style="list-style-type: none"> ATA/ATAPI-5 standard compliant host UDMA-66 transfer speed capabilities (66 MB/s max transfer speed) RX and TX FIFOs for data transfer through the Core DMA/UDMA and PIO data transfers supported Dedicated signal for polling ATA-device status Dedicated signal for executing Software Reset command Two Clock domains: Core Clock and System Clock domains Dedicated system side input bus for writing data to the ATA device Dedicated system side output bus for data read from the ATA device Required Core Clock Speed: 100MHz Available PIO Modes: 0 and 4 Number of ATA devices supported on the IDE Bus: 1 <p>Target Device Families: Spartan 3/3E, Virtex-II/IIPro/4</p> <ul style="list-style-type: none"> Number of Slices: 911 Number of Memory Bits: 8192 <p>ISE Version: 6.2i</p>	<ul style="list-style-type: none"> Check Power Mode Identify Device Idle Idle Immediate Initialize Device Parameters Read Verify Sector(s) Seek Set Features Set Multiple Mode Sleep Standby Standby Immediate Execute Device Diagnostic Read DMA Read Multiple Read Sector(s) Write DMA Write Multiple Write Sector(s)

System Architecture



Nuvation ATA-5 / UDMA-66 IDE Core Architecture for Xilinx Devices

ATA I/O Signal List



The following table lists I/O signals for the ATA Core. Input and output directions are with respect to the ATA Core.

Internal Signal Name	I/O	Description
General Signals		
core_clk	I	ATA Core Global Clock (TBD MHz)
core_reset_n	I	ATA Core Global Reset
ATA Bus		
CS0_n	O	Chip Select 0
CS1_n	O	Chip Select 1
DD[15:0]	I/O	Data Bus
DASP_n		Device active or slave present
DA[2:0]	O	Device Address
DMACK_n	O	DMA Acknowledge
DMARQ	I	DMA Request
INTRQ	I	Interrupt Request
DIOR_n	O	3 purpose signal: - I/O read - DMA ready during Ultra DMA data in bursts - Data strobe during Ultra DMA data out bursts
IORDY	I	3 purpose signal: - I/O ready - DMA ready during Ultra DMA data our bursts - Data strobe during Ultra DMA data in bursts
DIOW_n	O	Dual Purpose Signal: - I/O write - Stop during Ultra DMA data bursts
PDIAG_n		Dual Pupose Signal: - Passed diagnostics - Cable assembly type identifier
RESET_n	O	Reset
Local Side Interface		
General Signals		
sys_clk	I	System-side (User) Clock
sw_reset	I	Signal is asserted to initiate a software reset of the device.
read_all_status	I	A 0-to-1 transfer initiates a read of all current status registers. Must be re-set to 0 again before a subsequent 'read all status' request.
core_busy	O	This signal indicates the Core's current status - whether it is busy or idle.
Input ATA Transactions		
Command Path (control path)		
feature[7:0]	I	Feature field of the task file (command block)
sector_count[7:0]	I	Sector Count field of the task file
sector_number[7:0]	I	Sector Number field of the task file
cylinder_low[7:0]	I	Cylinder Low field of the task file
cylinder_high[7:0]	I	Cylinder High field of the task file

Internal Signal Name	I/O	Description
device_head[7:0]	I	Device Head field of the task file
command_dav	O	When high, the ATA Core can accept a new command
command[7:0]	I	Command field of the task file
command_valid	I	Initiates the Command. Qualifies the following buses: feature, sector_count, sector_number, cylinder_low, cylinder_high, device_head, command and transaction_id_in
transaction_id_in[3:0]	I	User Field for identifying various transactions. This value will be returned to the user on the "transaction_id_out" bus when the command has been processed. [for future use]
command_error	O	This signal is high for one cycle after an unsupported command is dispatched or if the core receives a new command when it is busy.
cp_op_code[7:0]	I	Command Packet Op Code. This field is validated with the command_valid. The command packet should be available at the same time that Task File register command is dispatched. [for future use]
cp_logical_block_address[31:0]	I	Command Packet Logical Block address field: Bits 31 to 24 correspond to Byte 2 of command packet. Bits 23 to 16 correspond to Byte 3. Bits 15 to 8 correspond to Byte 4. Bits 7 to 0 correspond to Byte 5. This field is validated with the command_valid. [for future use]
cp_logical_unit_number[2:0]	I	Command Packet Logical Unit Number [for future use]
cp_length_field[15:0]	I	Command Packet Length field: Bits 15 to 8 correspond to Byte 7 of command packet. Bits 7 to 0 correspond to Byte 8. This field is validated with the command_valid. [for future use]
Input Data Path (data path)		
sector_data_in_dav	O	Core can accept sector data
sector_data_in_valid	I	Input Data is Valid
sector_data_in[15:0]	I	Data to be written to the storage media (qualified by sector_data_valid)
sector_data_overflow	O	This signal is asserted for every cycle that data was lost in the sector_data FIFO.
Output ATA Transactions		
Status Path (control path)		
error[7:0]	O	Error Field of command results
status_sector_count[7:0]	O	Sector Count field of the task file (if required)
status_sector_number[7:0]	O	Sector Number field of the task file (if required)
status_cylinder_low[7:0]	O	Cylinder Low field of the task file (if required)
status_cylinder_high[7:0]	O	Cylinder High field of the task file (if required)
status_device_head[7:0]	O	Device Head field of the task file (if required)
status[7:0]	O	Status Field of command results
status_valid	O	This signal indicates when the appropriate status signals are valid. [for future use]
transaction_id_out[3:0]	O	When valid, this signal contains the same value that was placed on the "transaction_id_in" bus upon command initiation.
Output Data Path (data path)		
sector_data_out_dav	O	When high, this signal indicates whether there is data available for the user to read.
sector_data_out_ena	I	When high, and if data available, this signal causes data to be placed on the "sector_data_out" bus on a cycle-by-cycle basis.
sector_data_out_valid	O	This signal qualifies the following bus: sector_data_out
sector_data_out[15:0]	O	The data read from storage media

NOTE: The Nuvation ATA-5 IP Core can be customized to customer requirements. For example, the signal list may be altered to support extra functionality provided by ATAPI commands for a Packet interface / Packet command.