



HIGHLIGHTS

- Supports up to 16 analog video channel inputs
- Utilizes four TVP5154 quad-channel low power video decoders with independent scalers
- Low-cost Xilinx Spartan-3A FPGA streaming to a TI DM6467 DVEVM (Digital Video Evaluation Module) based on DaVinci™ technology
- Intended for evaluation use with TI's DM6467 DVEVM to add multichannel video input capability

OVERVIEW

Nuvation's Multichannel Video Front End (McVFE) is a reference design that merges up to 16 video streams for encoding in TI DaVinci™ devices. McVFE is geared for evaluation and rapid development of multichannel video encoders and video servers based on low-cost Xilinx FPGAs with TI TVP Decoders and DaVinci™ technology. **NOTE: The TI DM6467 DVEVM must be purchased separately.**

ON-BOARD DEVICES

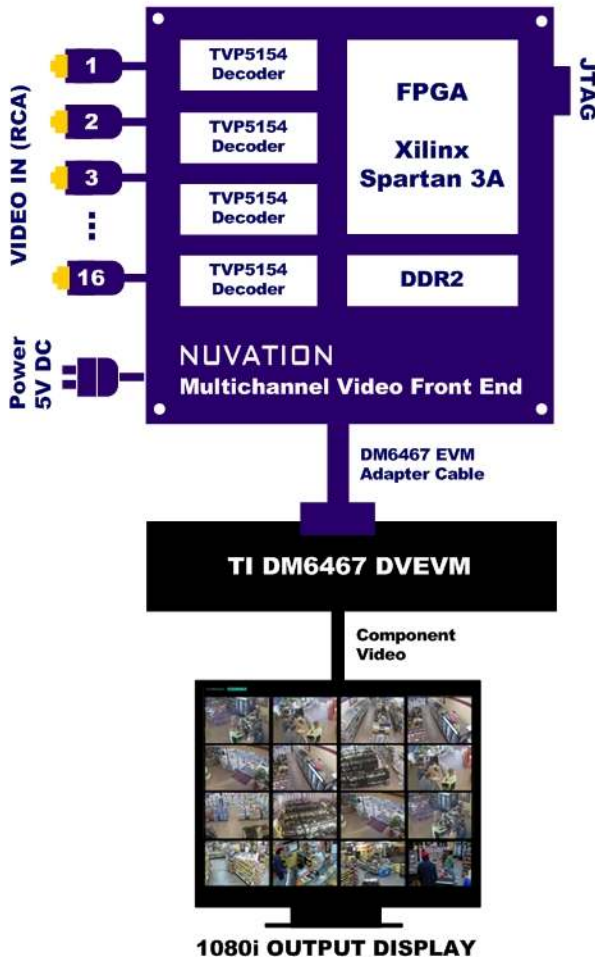
- 4 TI TVP5154 video input decoders for NTSC video decoding with independent scalers for up to 16 channels. PAL/SECAM support available as add-on.
- Xilinx Spartan 3A FPGA, XC3S700A-5FGG400
- 16-bit, 256Mb DDR2 memory interface at 133MHz
- SPI Flash and hard reset button for auto boot up configuration. The FPGA can also be configured by the DM6467 firmware application, which is the normal mode of operation.

INTERFACES

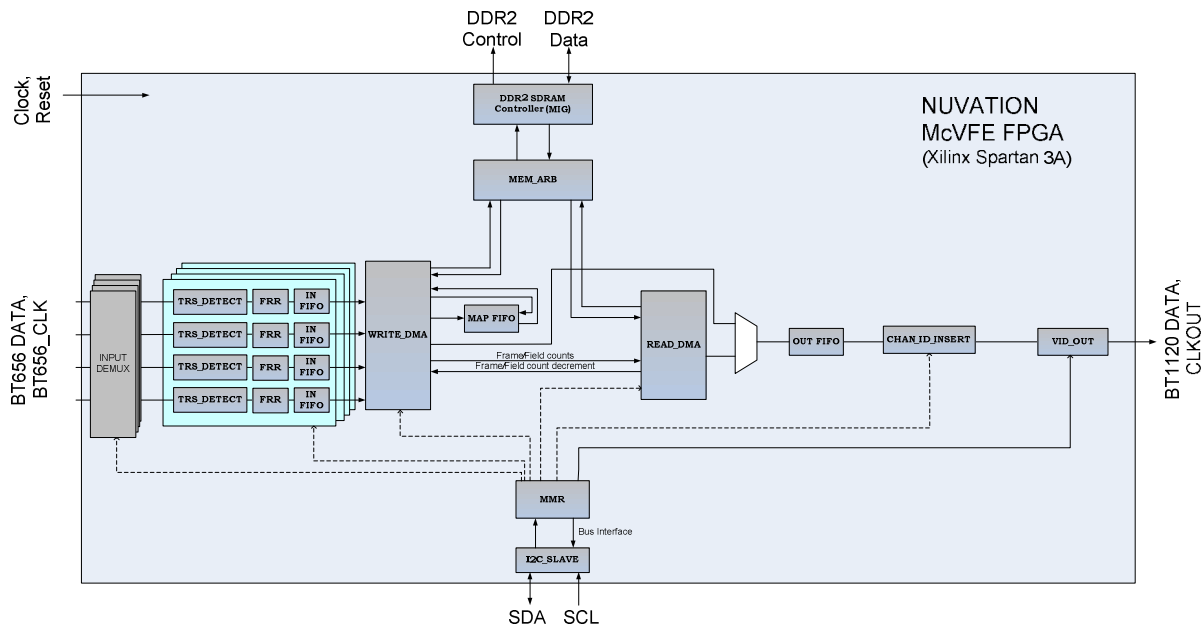
- **16 RCA IN:** 16 NTSC video inputs with an optional anti-aliasing filter per input. Contact Nuvation to support other video standards.
- **I²C:** When connected, the DM6467 EVM is the I²C master and all I²C ports on the McVFE board are slaves. In stand alone mode, the McVFE Xilinx FPGA is the I²C master
- **DM6467 EVM Cable Adapter:** Cable and adapter board to connect to TI DM6467 DVEVM
- **LEDs:** For power and general purpose display (FPGA programmable)
- **JTAG:** Compatible with the Xilinx Platform cable USB (HW-USB-G)
- **Power connector:** External AC/DC power adapter (included) supplies 5V

FIRMWARE

- FPGA programming driver
- Video for Linux 2 (v4l2) accessible McVFE driver
- Embedded Linux demo application to display the individual video streams on a 1080i display
- Linux kernel patch
- Firmware supports frame mode only



Nuvation McVFE System Diagram



FPGA THEORY OF OPERATION

- The Xilinx Spartan 3A FPGA on the McVFE board takes 16 independent asynchronous BT.656 video inputs and concatenates them into a single BT.1120 video output.
- The FPGA has two modes of operation:
 - Frame mode: The unit of data to be buffered is an entire frame
 - Field mode: The unit of buffered data is a field
- The BT.1120 video output from the FPGA is sent to a TI DaVinci™ DM6467 DSP on the TI DM6467 DVEVM board, using a 16-bit capture port. The design is parameterized to support a wide range of target applications with either a single 8-bit or 16-bit video capture port.
- Input channels are independently decoded. All data between SAV and EAV is preserved in memory to save any ancillary data in the VBI. Channels are then read from memory and sent to the output port, sequenced on a priority basis.

PACKAGE CONTENTS

- McVFE printed circuit board (Board Dimensions: 6.5" x 7.5")
- DM6467 EVM Cable Adapter
- Samtec HFEM2-020-T-05.00-SE Flex cable
- 5V DC universal power supply (100-240V, 50-60Hz) with North American 110V AC-plug
- Firmware for TI DM6467 DVEVM
- Quick Start User's Guide

DEMO APPLICATION

- The DM6467 firmware demo application loads the FPGA bitstream during initialization and programs registers in the McVFE FPGA and TVP5154 devices via I²C commands. It then configures the Video Port Interface (VPIF) in the DM6467 DSP to capture the video stream coming from the FPGA.
- During normal operation, for every frame of video that is captured, the demo application searches the capture buffer for a vertical ancillary packet (SMPTE 291 compliant) at a known location that identifies the channel index for that frame. It then copies (using DMA) the active video from the input capture buffer to the corresponding region in the output display buffer.
- The demo application supports frame mode only.
- NOTE: When using 16 input channels, the TVP5154 devices on the McVFE board scale the active video by a factor of two both horizontally and vertically, and add horizontal blanking between lines to maintain the same line-rate.

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