

Serial ATA Host Controller IP Core for Altera Devices

The Nuvation SATA Host Controller IP Core is a drop-in core used to interface between memory or memory mapped I/O and SATA devices. The core includes the transport and link layers of a host controller, or host bus adapter (HBA) and is fully compliant the SATA 2.6 specification at 1.5Gbps or 3Gbps. The core is compliant with the Serial ATA Advanced Host Controller Interface (AHCI) v1.3 specification. AHCI is a native Serial ATA interface that simplifies the HBA down to a data-mover, while providing a clean mechanism for command queuing. The Nuvation SATA core features an Avalon interface for easy integration in SOPC Builder environments.

Nuvation’s SATA Host Controller IO core is used frequently in applications that require an FPGA and also require r/w to SATA storage devices. Implementing SATA in spare FPGA resources can reduce PCB real estate and product cost. Medical Devices, Defense, Aerospace, Video Security, Scientific Instrumentation, and other markets are common users of Nuvation storage IP cores. Nuvation’s SATA Host Controller IP core can be implemented with multiple instantiations for RAID-type applications. It can also be implemented in conjunction with external Port Multiplier devices.

The SATA Host Controller AHCI/Avalon requires an integrated Altera SERDES which supports SATA electrical requirements. Currently, Stratix® IV GX is available with such SERDES support. Arria® II GX is planned, pending characterization tests. When implemented in Altera Stratix® IV GX, migration to Altera HardCopy® IV ASIC is available.

The SATA IP core is available under Nuvation’s Core License Agreement (CLA). Licensee deliverables include encrypted Verilog source, Verilog Test Benches, NIOS II test software, detailed user guide (with screen shots, etc), email technical support, and a one year warranty. Unencrypted source code licenses, extended support, extended warranty programs, and design customization services are also available from Nuvation. ITAR, CGP, 510k, and other regulatory requirements can be supported. Altera has distinguished Nuvation as a premier Certified Design Center.

This Product Brief is for BETA RELEASE customers. General Availability (GA) is pending final design verification testing in licensee products. Please contact Nuvation for more information, ip@nuvation.com.

Features	
<ul style="list-style-type: none"> • Compliant to the Serial ATA AHCI 1.3 specification • 32 command slots per port, and 1 port per HBA • Supports both DMA and PIO protocols • 3 clock domains: system, link/transport layer, and receive • Out Of Band (OOB) signaling supported by Altera transceiver. • Spread-spectrum clocking (SSC) supported by Altera transceiver. • Avalon bus interface, integrated into SOPC Builder • 32-bit internal buses in link and transport layers • CONT primitive and “junk-data” scrambler to reduce EMI • FIFOs between each architecture layer <ul style="list-style-type: none"> ○ Shallow link-phy FIFOs for phase/frequency variations in external PHY ○ Shallow transport-link FIFOs for flow control and temporary storage ○ Deep DMA controller FIFOs for data-rate matching • Supports native command queuing • Supports command-list override • Supports PIO multiple DRQ Block • Supports auto-speed negotiation • Support for FIS Switching, Async Notification, HotPlug, and other optional extensions to the SATA 2.6 specification available through customization services. 	
Target Device Families: Altera Stratix IV GX	
• Number of Combinatorial ALUTs:	4,000
• Number of Memory ALUTs:	200
• Number of Registers:	3,500
• Number of Block Memory Bits:	38,912 (6 M9Ks)

SATA Host Controller IP Core Architecture

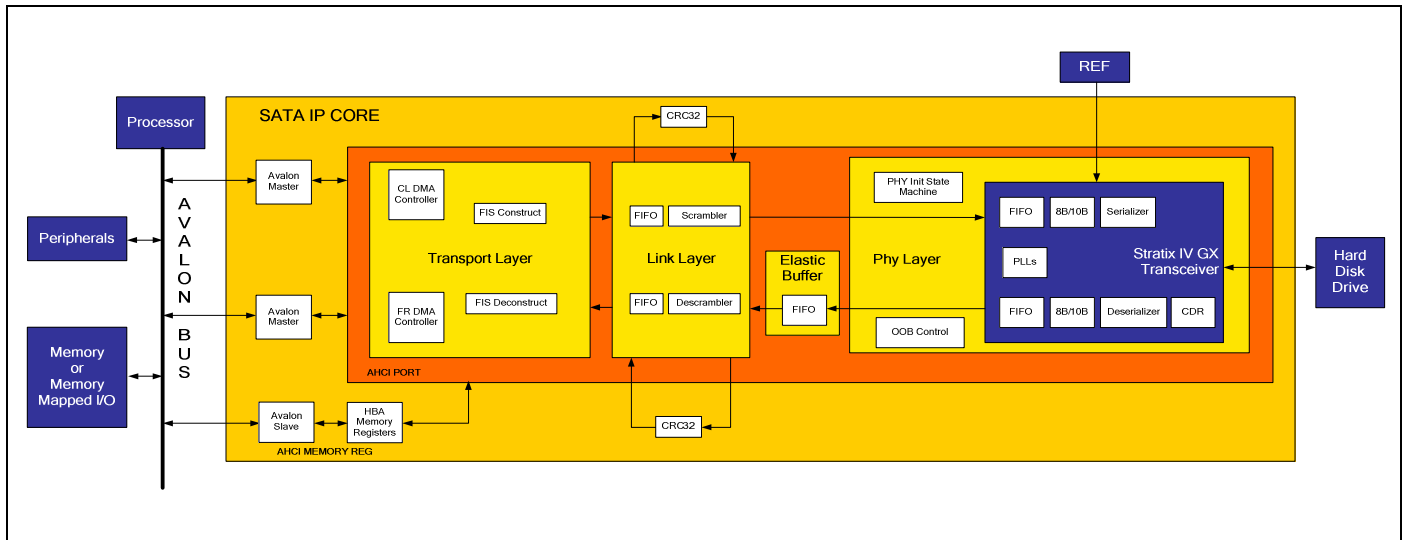


Figure 1: Nuvation SATA Host Controller IP Core Architecture for Altera Stratix IVGX

SATA Host Controller SoC Implementation Example

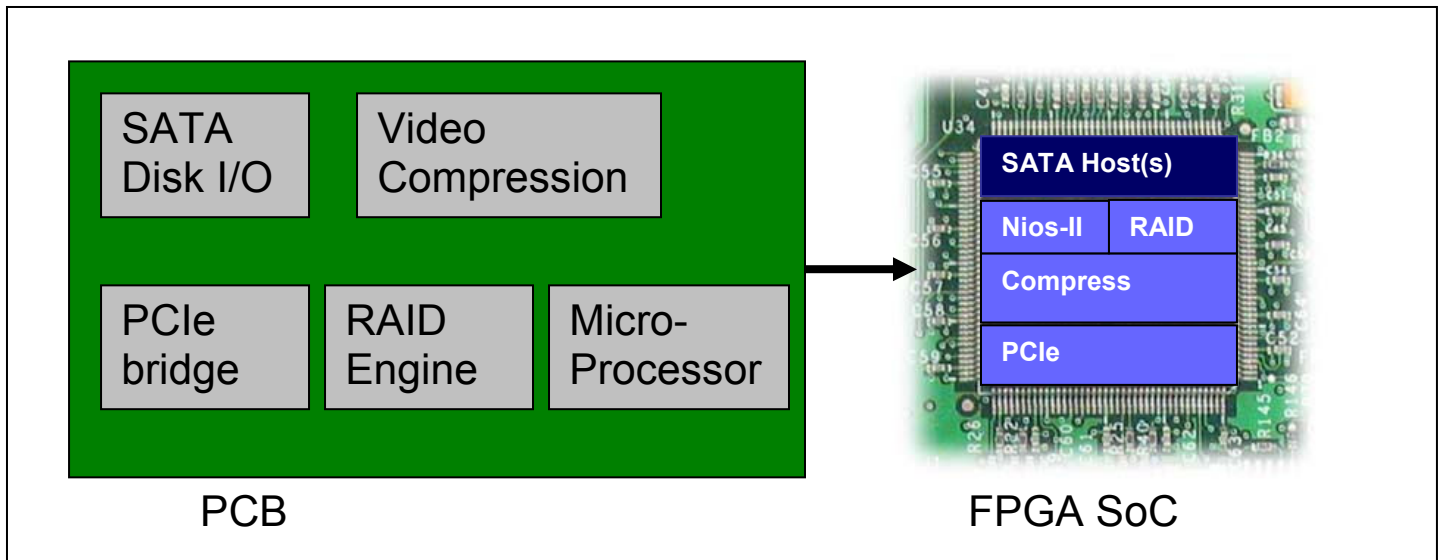


Figure 2: FPGA SoC Implementation Example

SATA I/O Signal List

The following table lists I/O signals for the SATA Core. Input and output directions are with respect to the core.

Internal Signal Name	I/O	Description
iRESET	I	Reset: Active high, system reset. Assumed to be synchronized to SYS_CLK; the core will synchronize iRESET to each clock domain as required.
iSYS_CLK	I	Clock: System clock, completely independent of the communication link. Usually matches the frequency of the memory subsystem.
iPLL_CLK	I	Clock: Transceiver reference clock. Must be exactly 150MHz.
iCAL_CLK	I	Clock: Transceiver calibration clock. Must be between 10MHz and 125MHz (pending characterization).
iRECONFIG_CLK	I	Clock: Transceiver reconfiguration clock. Must be between 37.5 MHz and 50 MHz.
iOOB_CLK	I	Clock: Clock used to measure and generate OOB signaling, Must be exactly 150MHz. Usually connected to the same source as iPLL_CLK.
oLT_DWORD_CLK	O	Clock: FPGA fabric-transceiver interface clock. 37.5MHz for Gen1 and 75MHz for Gen2.
iLT_DWORD_CLK	I	Clock: Internal clock domain used by the link and transport layers. Connect to oLT_DWORD_CLK.
oPHY_RCLK	O	Clock: In some devices, a PLL may be required to skew the recovered clock for timing closure. If not, then simply connect oPHY_RCLK to iPHY_RCLK. Refer to TBD for more information.
iPHY_RCLK	I	
oSATA_TX[0:0]	O	High Speed Serial: Output to Serial ATA device.
iSATA_RX[0:0]	I	High Speed Serial: Input from Serial ATA device.
iMR_CHIPSELECT	I	HBA Memory Registers: Active high chip select.
iMR_ADDRESS [12:2]	I	HBA Memory Registers: A word-address, unaligned access is not supported.
iMR_WRITE	I	HBA Memory Registers: Active high write enable.
iMR_WRITEDATA[31:0]	I	HBA Memory Registers: Write data.
iMR_BYTEENABLE [3:0]	I	HBA Memory Registers: Active high write byte-enables.
iMR_READ	I	HBA Memory Registers: Active high read enable.
oMR_READDATA[31:0]	O	HBA Memory Registers: Read data.
oMR_WAITREQUEST	O	HBA Memory Registers: Active high wait request, used to add peripheral controlled wait-states for clock synchronization between SYS_CLK domain and the internal clock domains.
oMR_IRQ	O	HBA Memory Registers: Active high interrupt request.
oMR_RESETPREQUEST	O	HBA Memory Registers: Reset Request. Asserted for one iPHY_RCLK cycle when an unsolicited COMINIT is detected. oMR_RESETPREQUEST should cause iRESET to be asserted to support asynchronous signal recovery.
oFR0_ADDRESS[31:0]	O	FIS Receive DMA: A byte address, but bits 1:0 will always be zero. Synchronous to SYS_CLK.
oFR0_WRITE	O	FIS Receive DMA: Active high write enable.
oFR0_WRITEDATA [31:0]	O	FIS Receive DMA: Write data.
iFR0_WAITREQUEST	I	FIS Receive DMA: Active high wait request.
oCL0_ADDRESS [31:0]	O	Command Layer DMA: A byte address, but bits 1:0 will always be zero.
oCL0_WRITE	O	Command Layer DMA: Active high write enable.
oCL0_WRITEDATA [31:0]	O	Command Layer DMA: Write data.
iCL0_WAITREQUEST	I	Command Layer DMA: Active high wait request.
oCL0_READ	O	Command Layer DMA: Active high read enable.
iCL0_READDATAVALID	I	Command Layer DMA: Read data valid.
iCL0_READDATA [31:0]	I	Command Layer DMA: Read data.
iENABLE_SIM_MODE	I	Simulation: Connect to '0'. Used for simulation purposes only.
iSIM_RX_SIGNALDETECT[0:0]	I	Simulation: Connect to '0'. Used for simulation purposes only.
oSIM_TX_FORCEECLIDLE[0:0]	O	Simulation: Leave unconnected. Used for simulation purposes only.
oDBG_RSVD [31:0]	O	Debug output: Reserved for future use.
oDBG_SENT_R_ERR[0:0]	O	Debug output: '1' for one oLT_DWORD_CLK cycle when the link-layer responded to a received FIS with an R_ERR primitive. '0' otherwise. Can be connected to a counter for packet error rate estimation.
oDBG_GOT_R_ERR[0:0]	O	Debug output: '1' for one oLT_DWORD_CLK cycle when the link-layer received an R_ERR primitive in response to a transmitted FIS. '0' otherwise. Can be connected to a counter for packet error rate estimation.
oDBG_CRC_ERR[0:0]	O	Debug output: '1' for one oLT_DWORD_CLK cycle when a CRC error is detected. '0' otherwise. Can be connected to a counter for packet error rate estimation.
oDBG_P0_CI[31:0]	O	Debug output: Connected to AHCI HBA register PxCI. Can be used to measure latency for a particular command in a way that excludes software overhead.
oDBG_P0_SACT[31:0]	O	Debug output: Connected to AHCI HBA register PxSACT. Can be used to measure latency of queued commands in a way that excludes software overhead.