

# Nuvation Signal Integrity Analysis

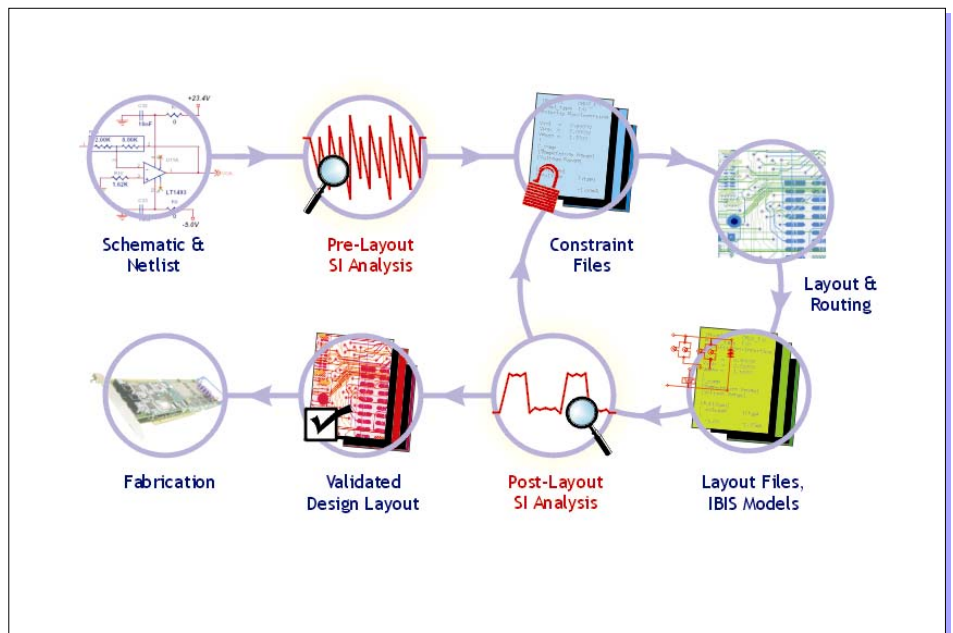


Can't afford a board re-spin?

Validate your board design before fabrication.

Designing a high-speed board? As PCB designs become more sophisticated, with higher clock speeds, higher device switching speeds, and higher density, the need to analyze signal integrity (SI) before prototyping is crucial.

Nuvation's Signal Integrity Analysis validates your design by applying digital and analog signal analysis to your schematic or layout to determine whether it will correctly propagate high-speed signals between components and connectors. Without SI Analysis, the trial and error approach can lead to endless rounds of board spins using various PCB materials and constraints, resulting in extensive debug time, prototyping expenses, and delays in product introduction.



## Services

Nuvation-SI consists of both pre-layout and post-layout analysis, ensuring optimal high-speed board layout and material selection.

**Pre-Layout Analysis:** In pre-layout analysis, your schematic and netlist are used to determine the optimum parts-placement, layout constraints, and design rules to be followed.

**Post-Layout Analysis:** In post-layout analysis, Nuvation will validate the quality of your layout, and simulate board functionality before fabrication. Nuvation utilizes IBIS models with the following tools:

## High-Speed Digital

(100MHz - 10GHz)

- Overshoot/Undershoot
- Impedance Matching
- Signal Slope Requirements
- EMI/EMC Analysis
- Ringing
- Bus Architecture
- Bypass/Decoupling Capacitors
- Board Delay & Timing
- Trace Separation
- Low-skew Clocking
- Fast Switching
- Cross-talk
- Ground Bounce
- Split Ground Planes
- Shielding

## Analog / RF

(50MHz - 40GHz)

- Noise Figure
- Substrate Noise
- Active Component Parameters
- Parasitic Coupling
- Width/Spacing/Length of Fingers
- Transmission Lines
- Grounded Transmission Line
- Discontinuities
- RF Signal Control
- Non-linear/Linear Noise of Non-linear Devices
- Optimization Limits
- Tuning to standard values
- EMI/EMC Analysis

## Tools

- Cadence® SPECCTRAQuest™
- Cadence® Allegro™
- Cadence® ORCAD and PSPICE
- Mentor® HyperLynx™
- Mentor® Expedition (VeriBest™)
- Mentor® PADS™
- Eagleware® GENESYS™

## Benefits

- Significantly reduce time for initial design analysis, constraints generation, full-board verification and bring-up
- Obtain board performance issues early in the design cycle
- Determine the optimum PCB material and parts placement
- Minimize EMI
- Save debug time, board spins, parts waste, and schedule slippage